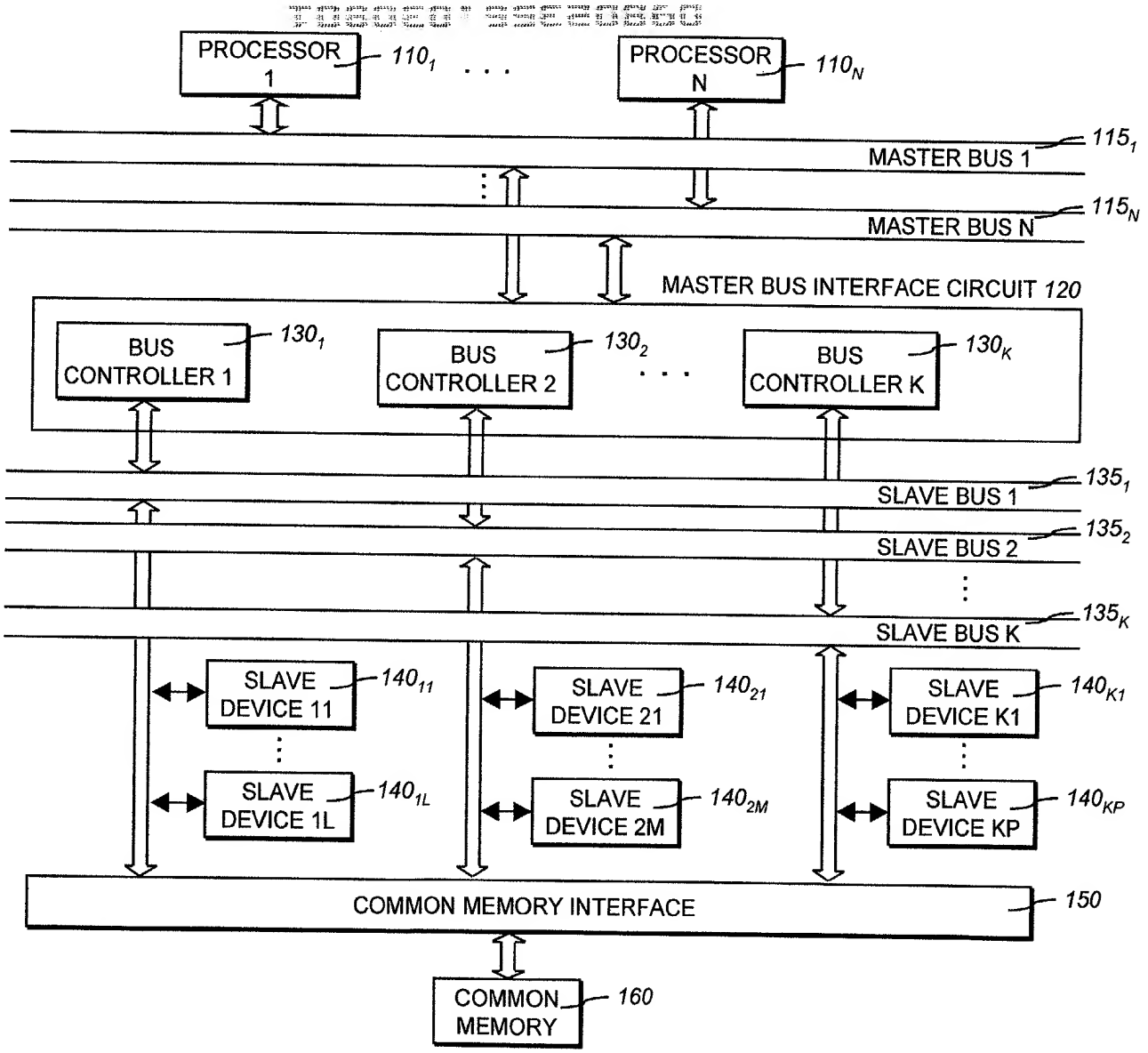
100
PROCESSOR 1
110$_1$
PROCESSOR N
110$_N$
MASTER BUS 1
115$_1$
MASTER BUS N
115$_N$
MASTER BUS INTERFACE CIRCUIT 120
BUS CONTROLLER 1
130$_1$
BUS CONTROLLER 2
130$_2$
BUS CONTROLLER K
130$_K$
SLAVE BUS 1
135$_1$
SLAVE BUS 2
135$_2$
SLAVE BUS K
135$_K$
SLAVE DEVICE 11
140$_{11}$
SLAVE DEVICE 1L
140$_{1L}$
SLAVE DEVICE 21
140$_{21}$
SLAVE DEVICE 2M
140$_{2M}$
SLAVE DEVICE K1
140$_{K1}$
SLAVE DEVICE KP
140$_{KP}$
COMMON MEMORY INTERFACE
150
COMMON MEMORY
160

FIG.1

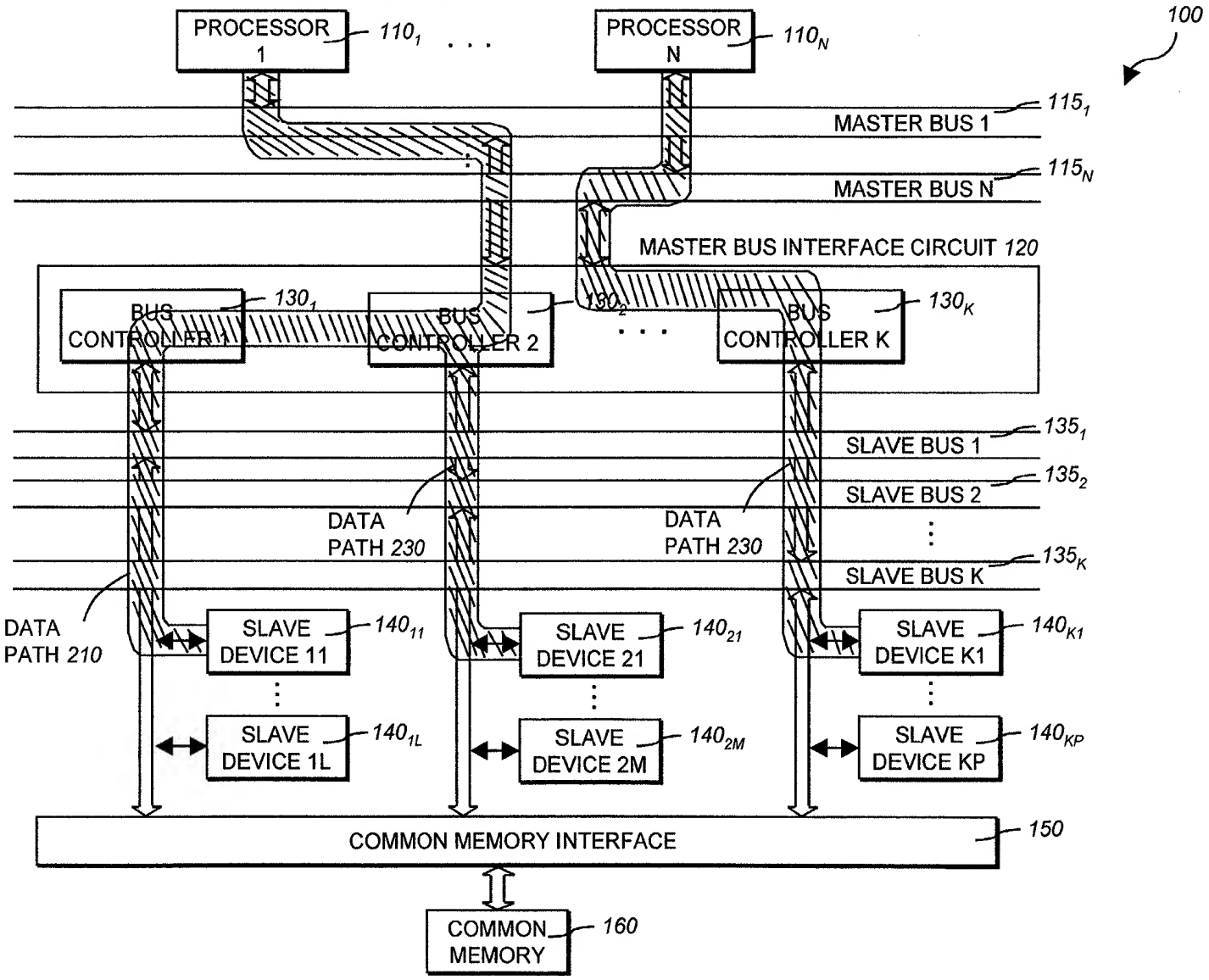
100
PROCESSOR 1
110$_1$
PROCESSOR N
110$_N$
115$_1$
MASTER BUS 1
115$_N$
MASTER BUS N
MASTER BUS INTERFACE CIRCUIT 120
BUS CONTROLLER 1
130$_1$
BUS CONTROLLER 2
130$_2$
BUS CONTROLLER K
130$_K$
135$_1$
SLAVE BUS 1
135$_2$
SLAVE BUS 2
135$_K$
SLAVE BUS K
DATA PATH 230
DATA PATH 230
DATA PATH 210
SLAVE DEVICE 11
140$_{11}$
SLAVE DEVICE 21
140$_{21}$
SLAVE DEVICE K1
140$_{K1}$
SLAVE DEVICE 1L
140$_{1L}$
SLAVE DEVICE 2M
140$_{2M}$
SLAVE DEVICE KP
140$_{KP}$
COMMON MEMORY INTERFACE
150
COMMON MEMORY
160

FIG.2A

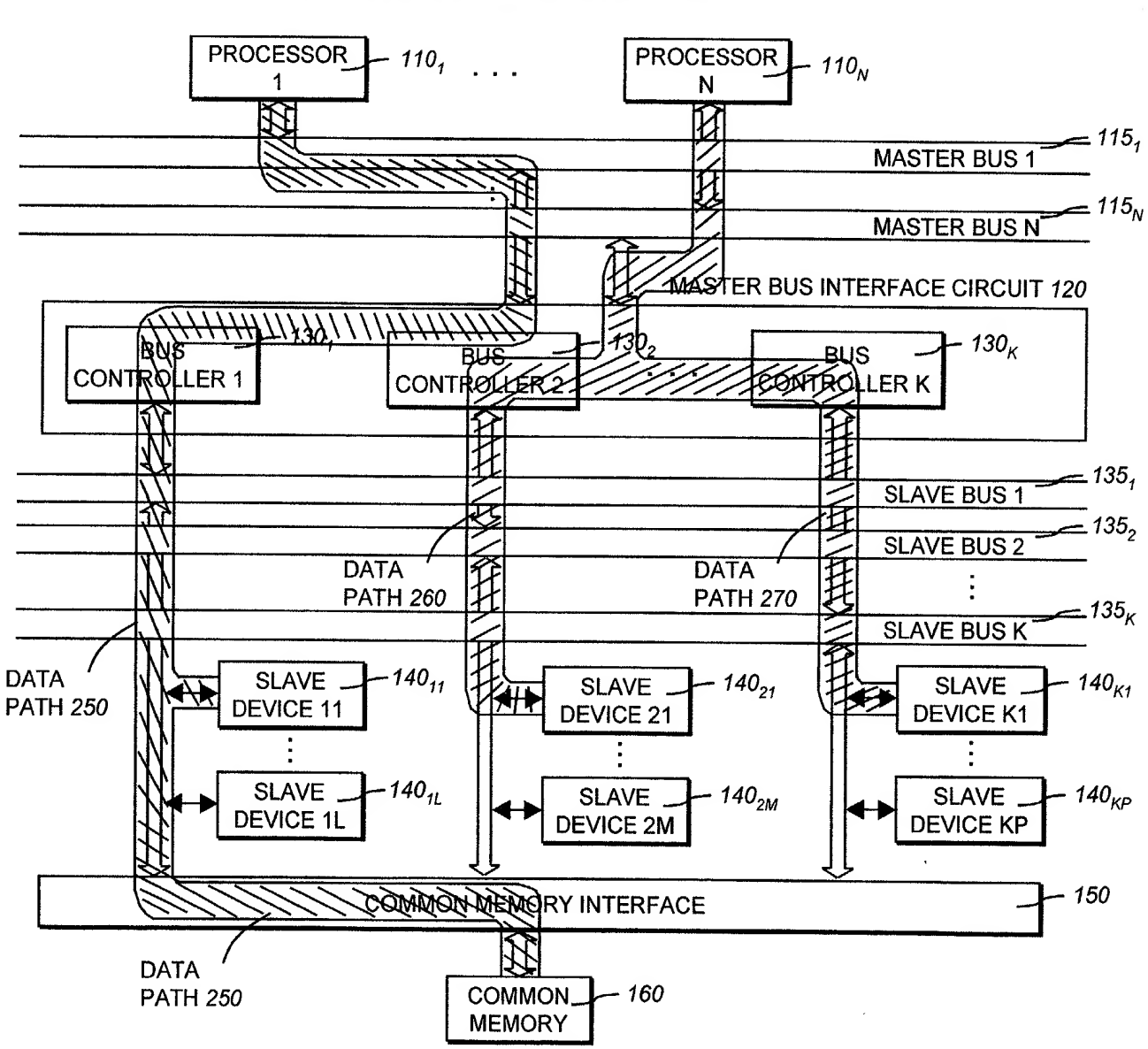
100
PROCESSOR 1
110$_1$
PROCESSOR N
110$_N$
115$_1$
MASTER BUS 1
115$_N$
MASTER BUS N
MASTER BUS INTERFACE CIRCUIT 120
BUS CONTROLLER 1
130$_1$
BUS CONTROLLER 2
130$_2$
BUS CONTROLLER K
130$_K$
135$_1$
SLAVE BUS 1
135$_2$
SLAVE BUS 2
135$_K$
SLAVE BUS K
DATA PATH 260
DATA PATH 270
DATA PATH 250
SLAVE DEVICE 11
140$_{11}$
SLAVE DEVICE 21
140$_{21}$
SLAVE DEVICE K1
140$_{K1}$
SLAVE DEVICE 1L
140$_{1L}$
SLAVE DEVICE 2M
140$_{2M}$
SLAVE DEVICE KP
140$_{KP}$
COMMON MEMORY INTERFACE
150
DATA PATH 250
COMMON MEMORY
160

FIG.2B

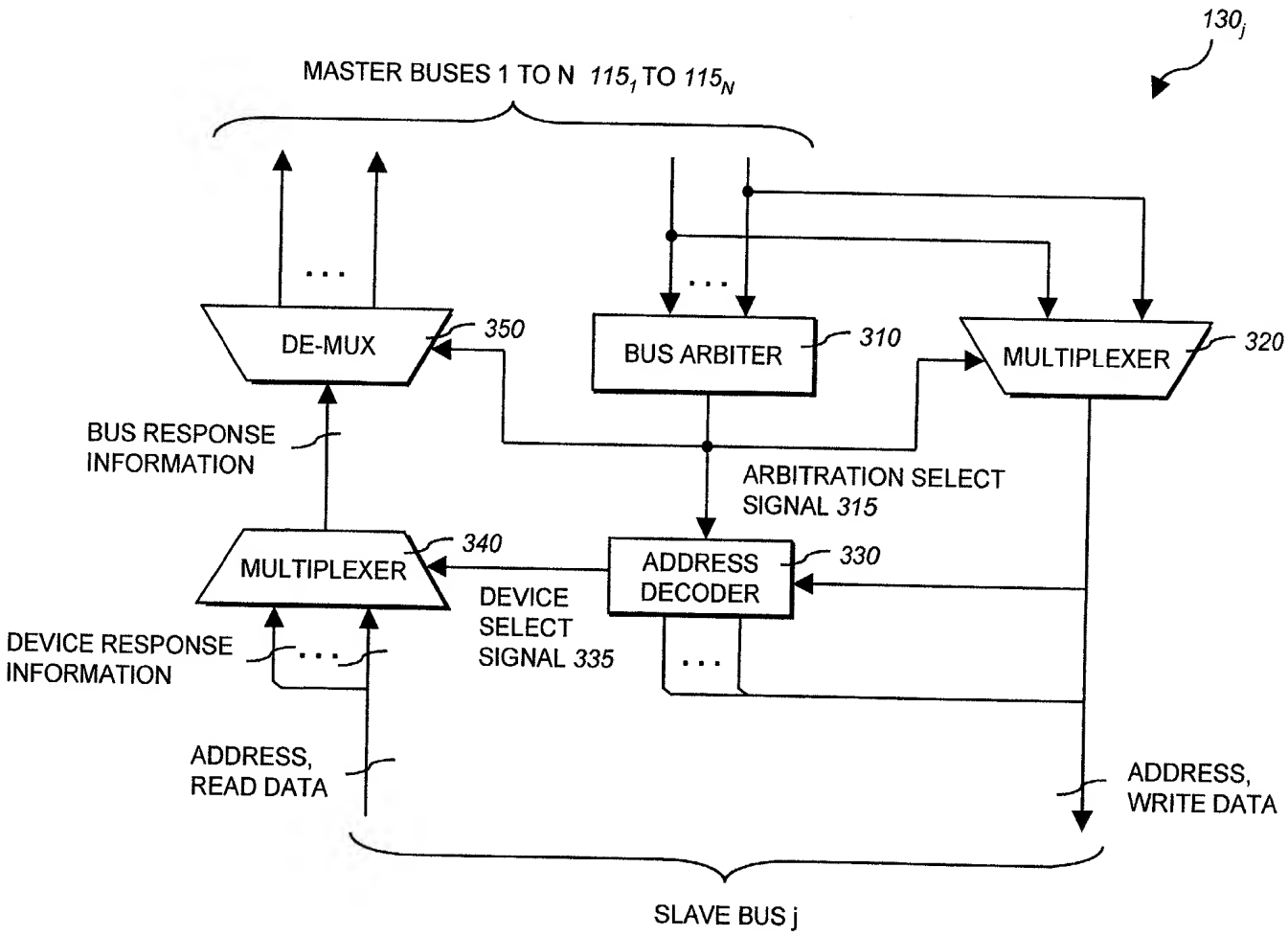
130j
MASTER BUSES 1 TO N 115₁ TO 115N
DE-MUX
350
BUS ARBITER
310
MULTIPLEXER
320
BUS RESPONSE INFORMATION
ARBITRATION SELECT SIGNAL 315
MULTIPLEXER
340
ADDRESS DECODER
330
DEVICE SELECT SIGNAL 335
DEVICE RESPONSE INFORMATION
ADDRESS, READ DATA
ADDRESS, WRITE DATA
SLAVE BUS j

FIG.3

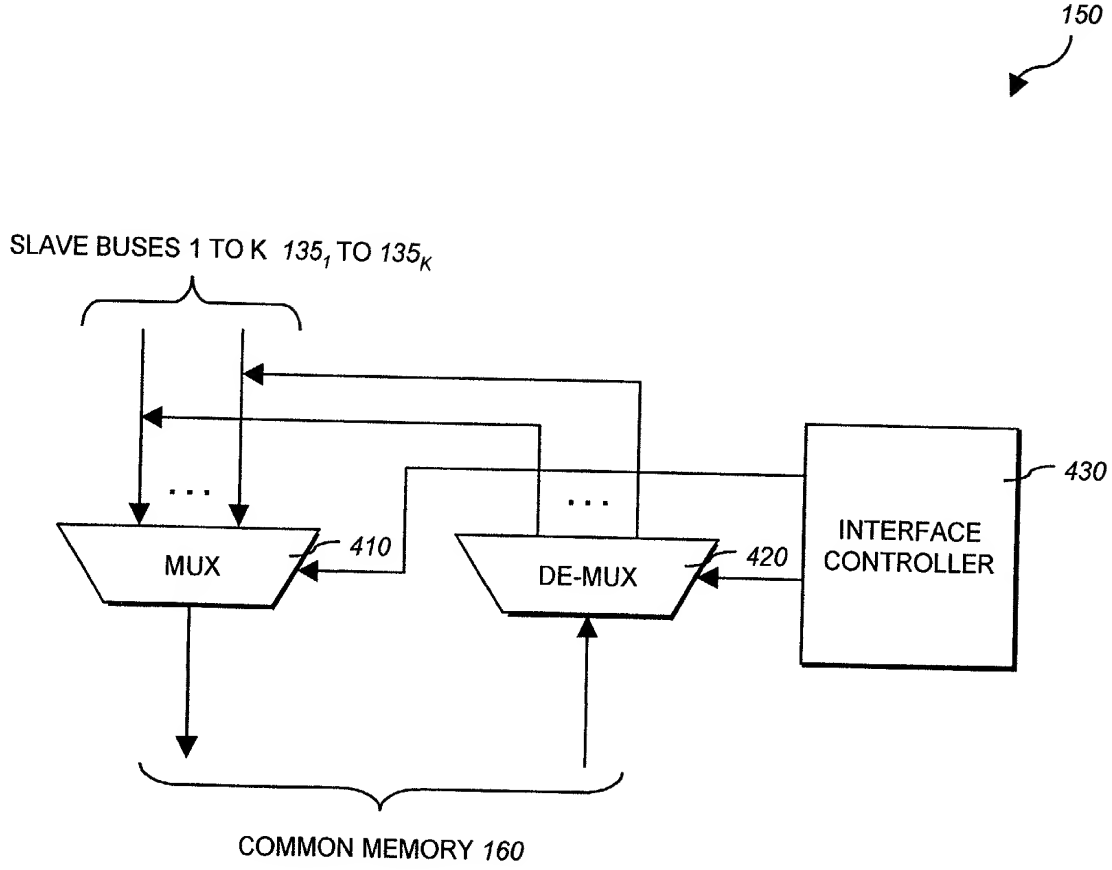
150
SLAVE BUSES 1 TO K 135$_1$ TO 135$_K$
MUX
410
DE-MUX
420
INTERFACE CONTROLLER
430
COMMON MEMORY 160

FIG.4